FIG. 1

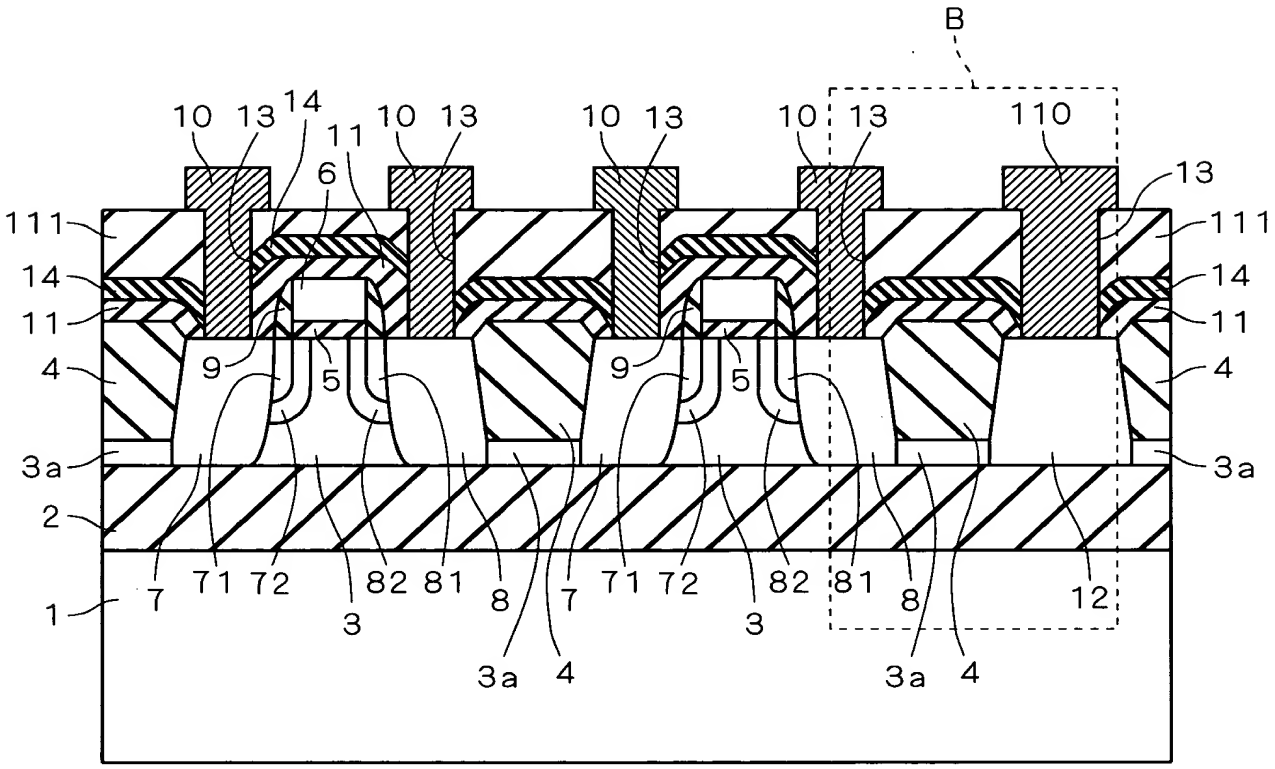
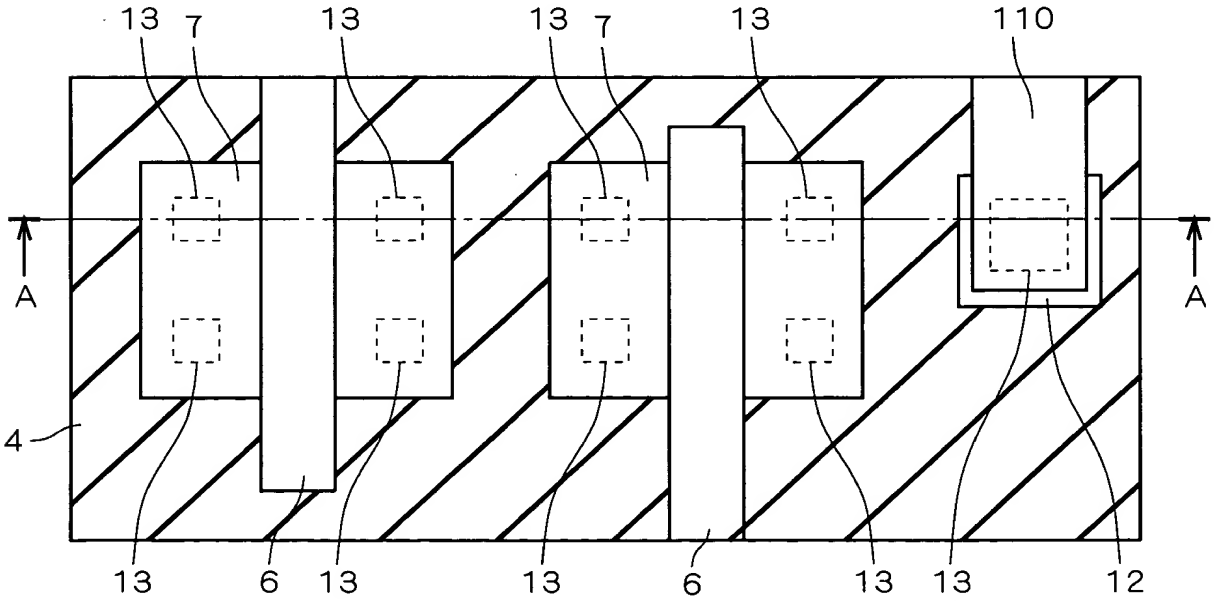


FIG. 2



F I G . 3

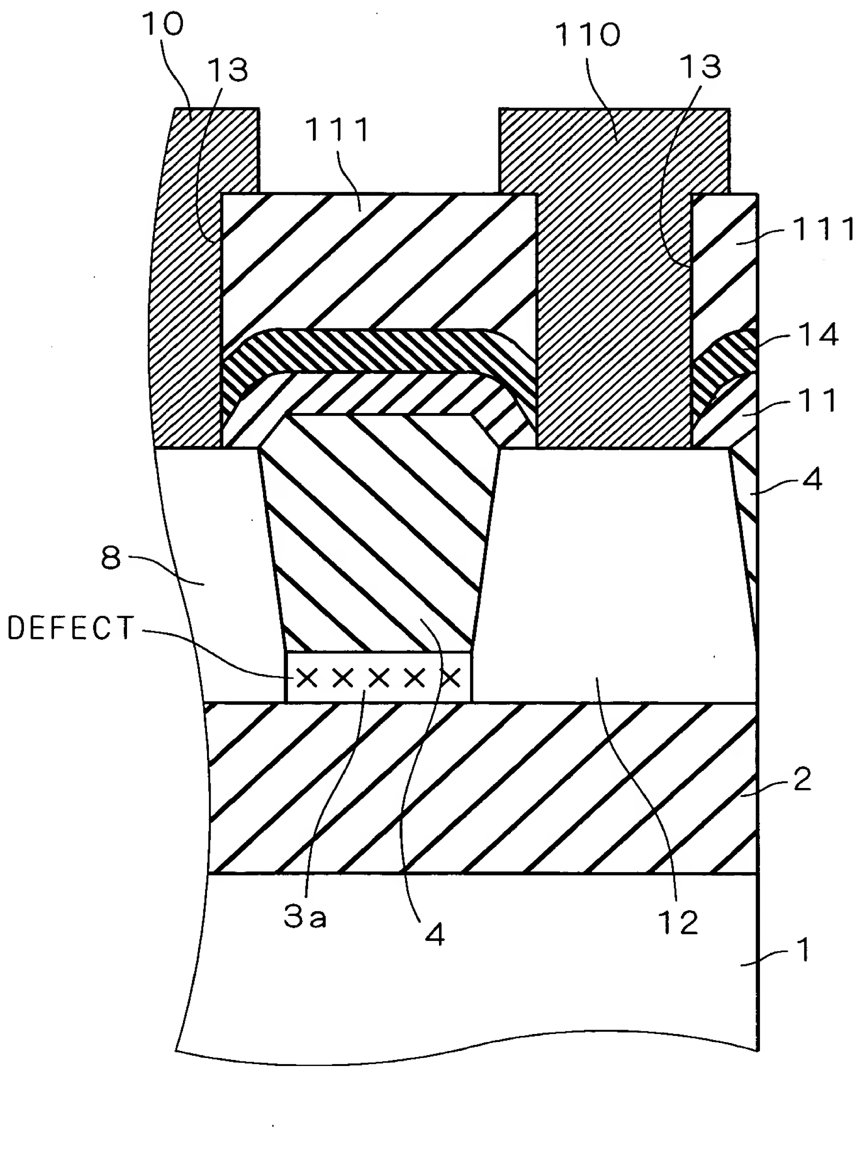
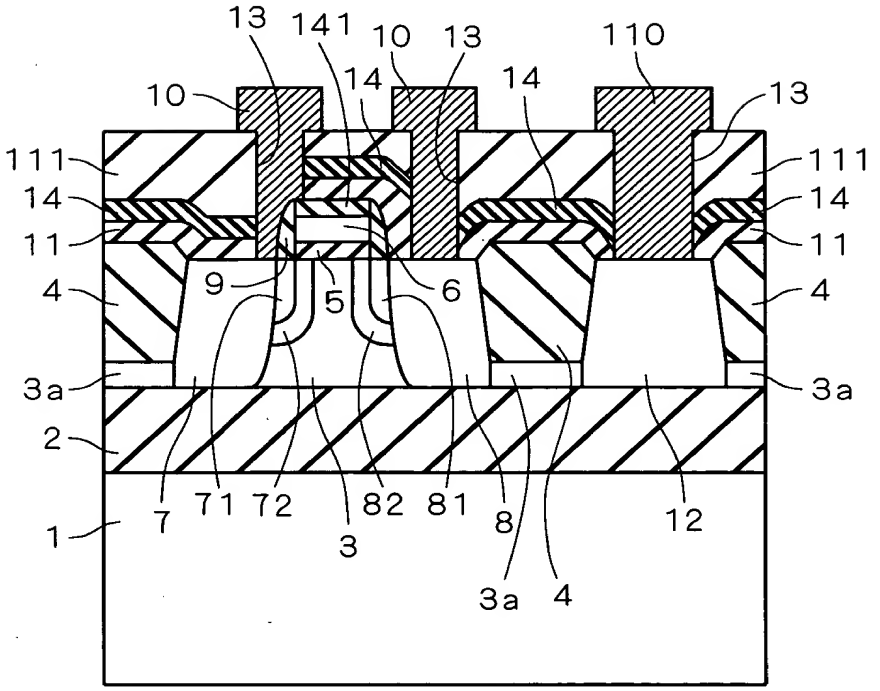


FIG. 4


13
141
10
13
110
10
14
14
13
111
111
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11
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9
5
6
4
3a
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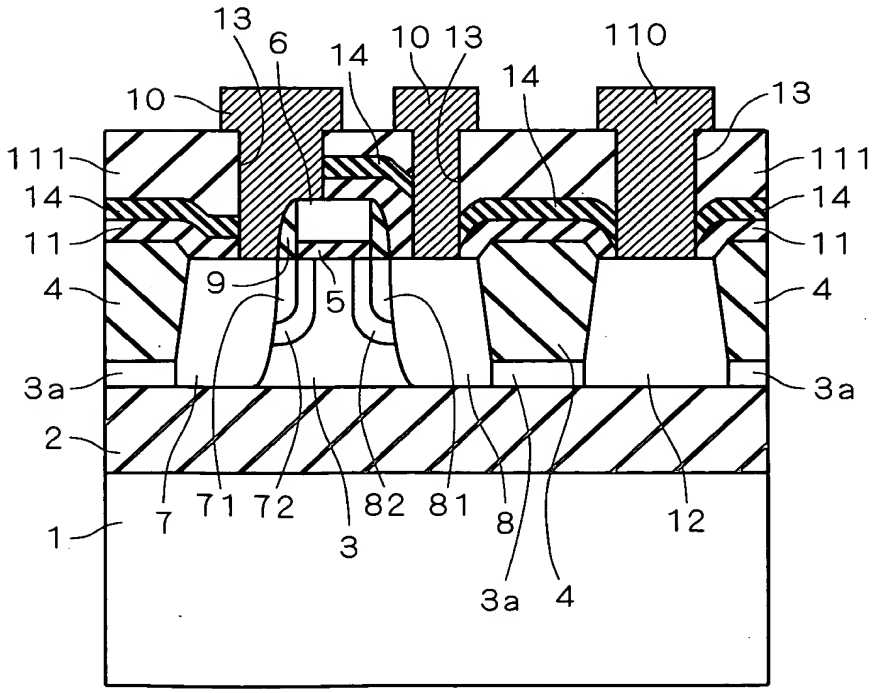
7
71
72
82
81
8
12
1
3
3a
4

FIG. 5


13
6
14
10
13
110
10
14
13
111
111
14
14
11
11
4
9
5
4
3a
3a
2
7
71
72
82
81
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3a
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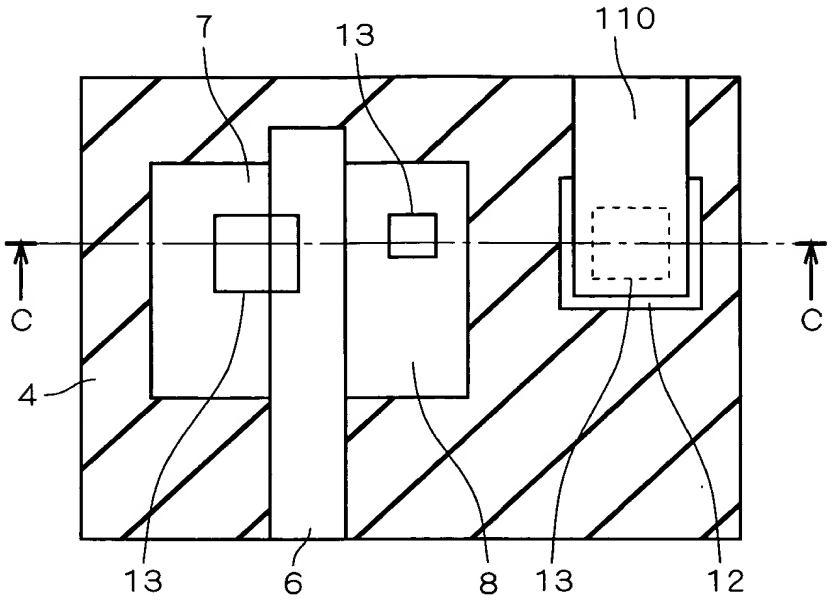
FIG. 6


7
13
110
C
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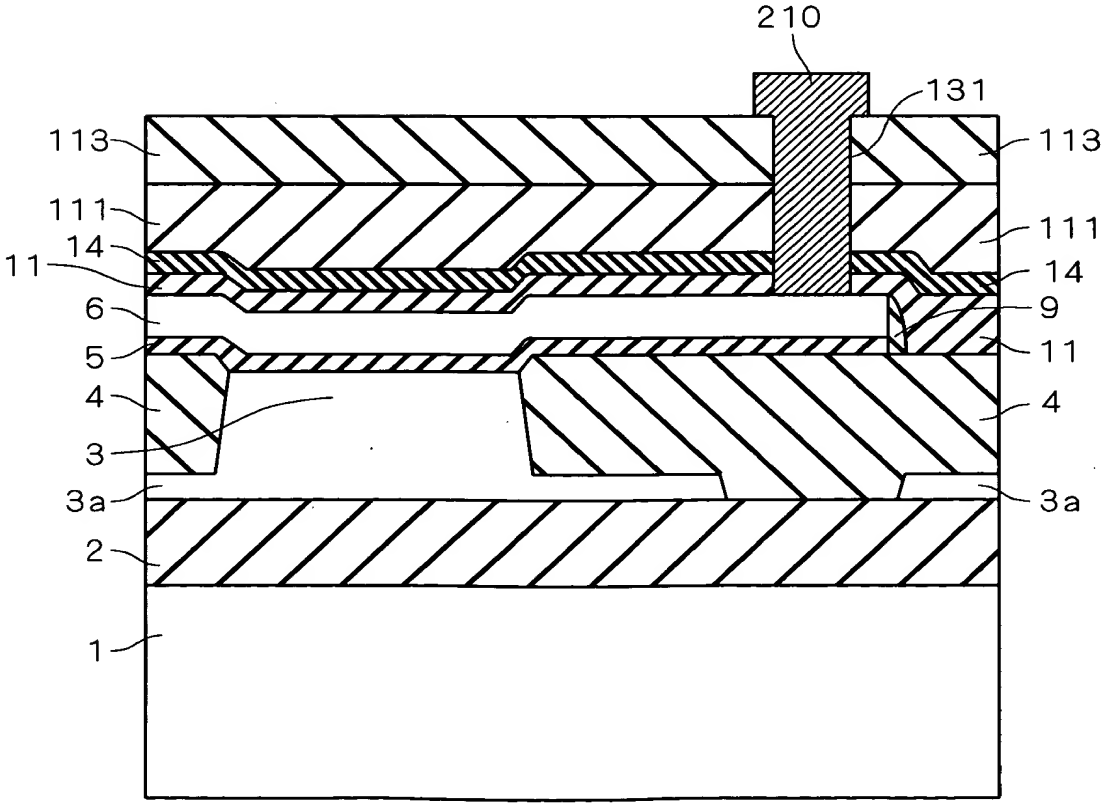
12

FIG. 7


210
131
113
113
111
111
14
14
11
6
9
5
11
4
4
3
3a
3a
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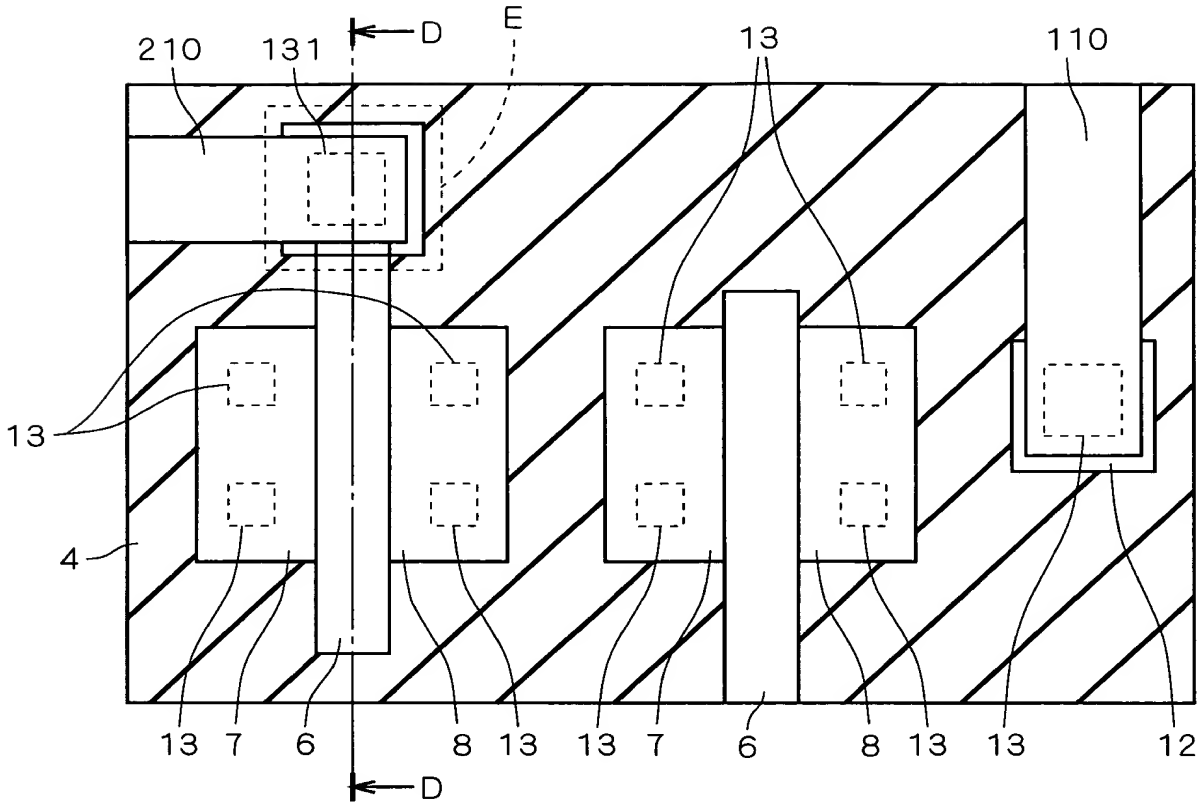
1

FIG. 8


210
131
D
E
13
110
13
4
13
7
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D

FIG. 9

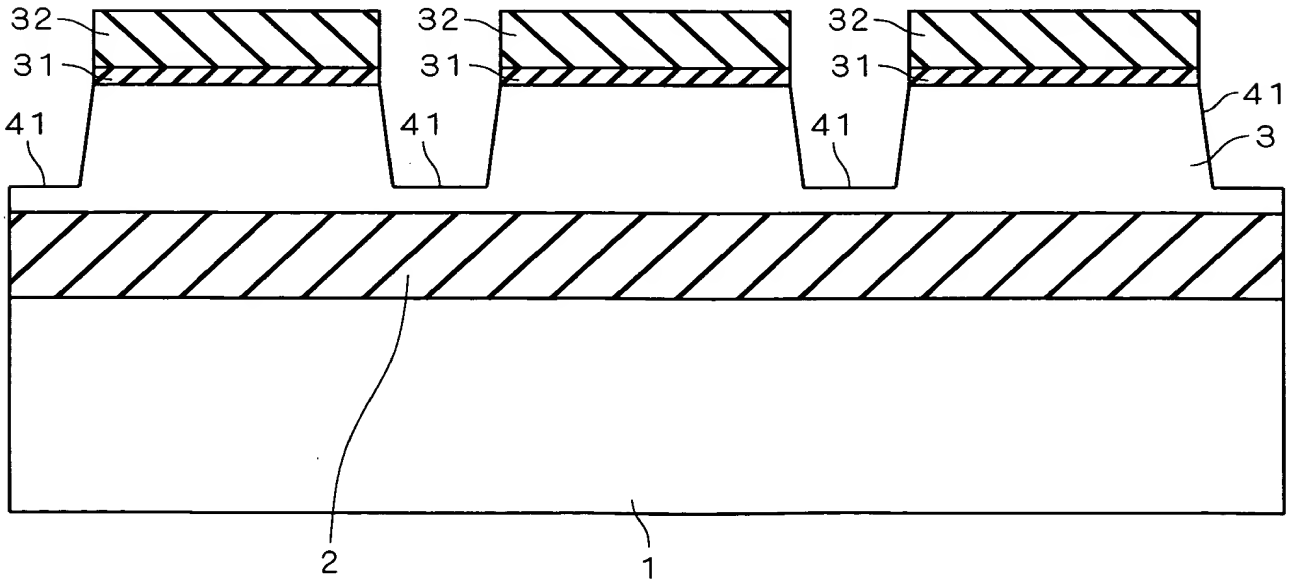
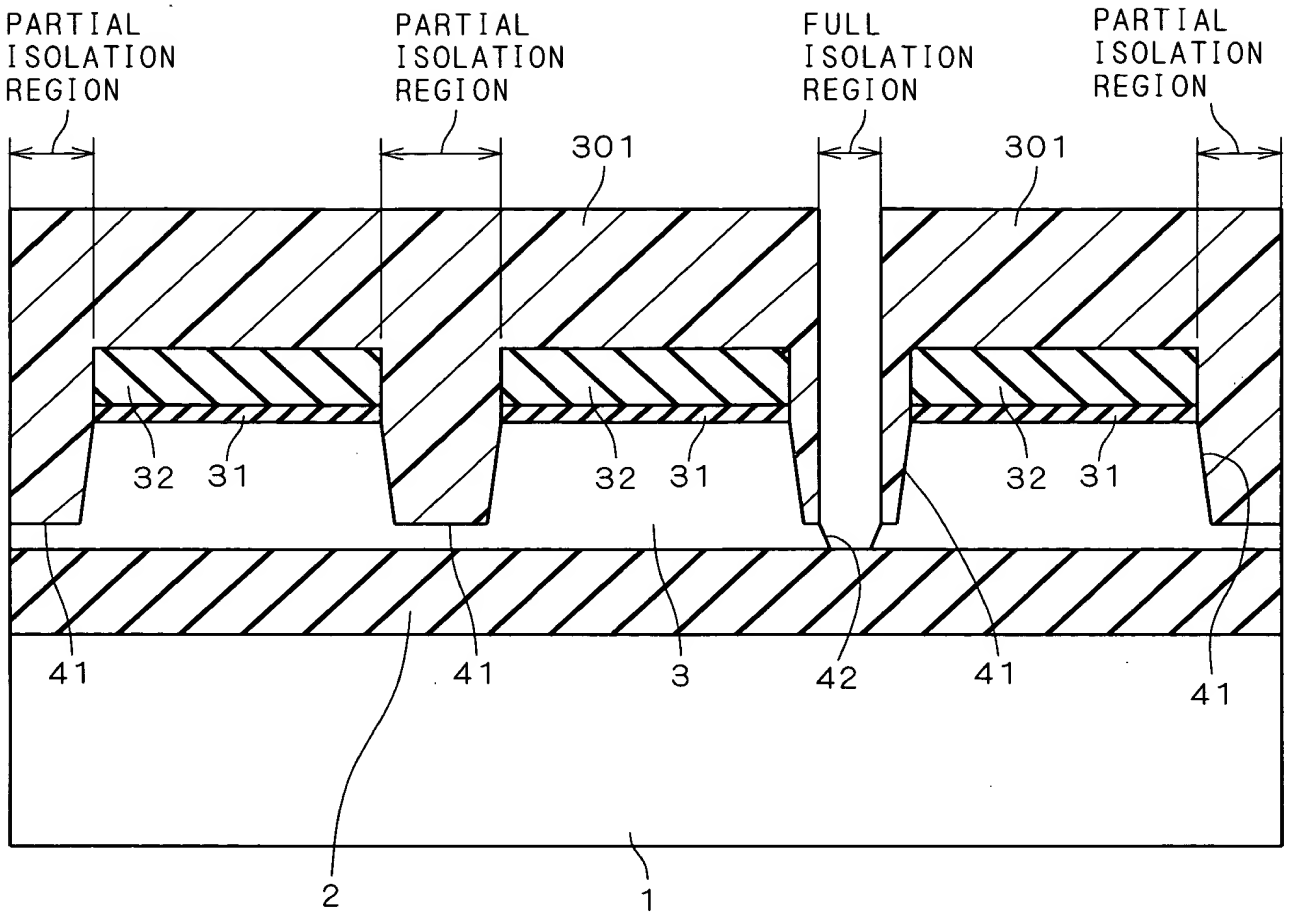

32
31
41
32
31
41
32
31
41
41
3
2
1

FIG. 10


PARTIAL ISOLATION REGION
PARTIAL ISOLATION REGION
FULL ISOLATION REGION
PARTIAL ISOLATION REGION
301
301
32
31
32
31
32
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42
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FIG. 11

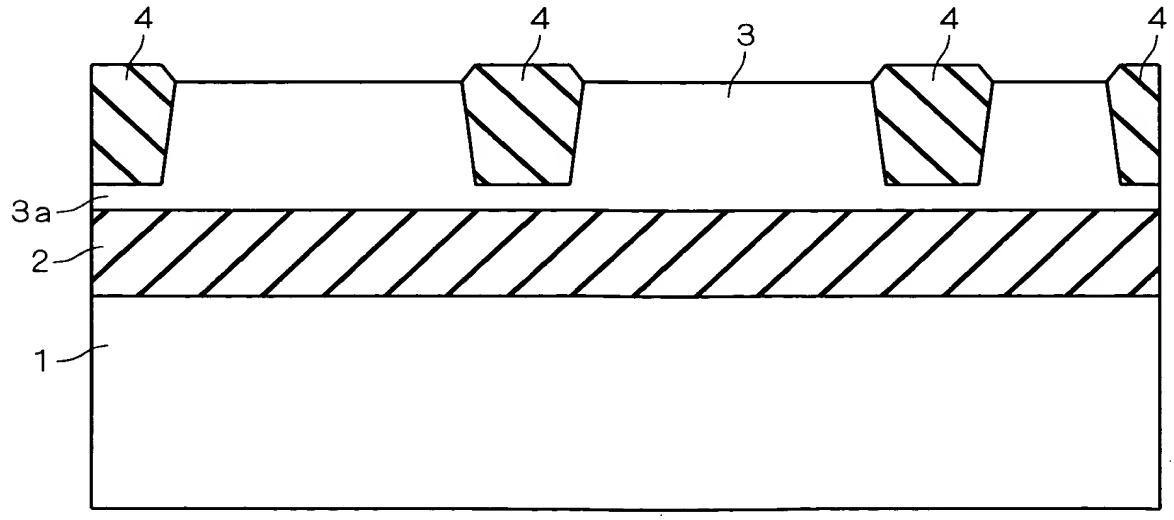

4
4
3
4
4
3a
2
1

FIG. 12

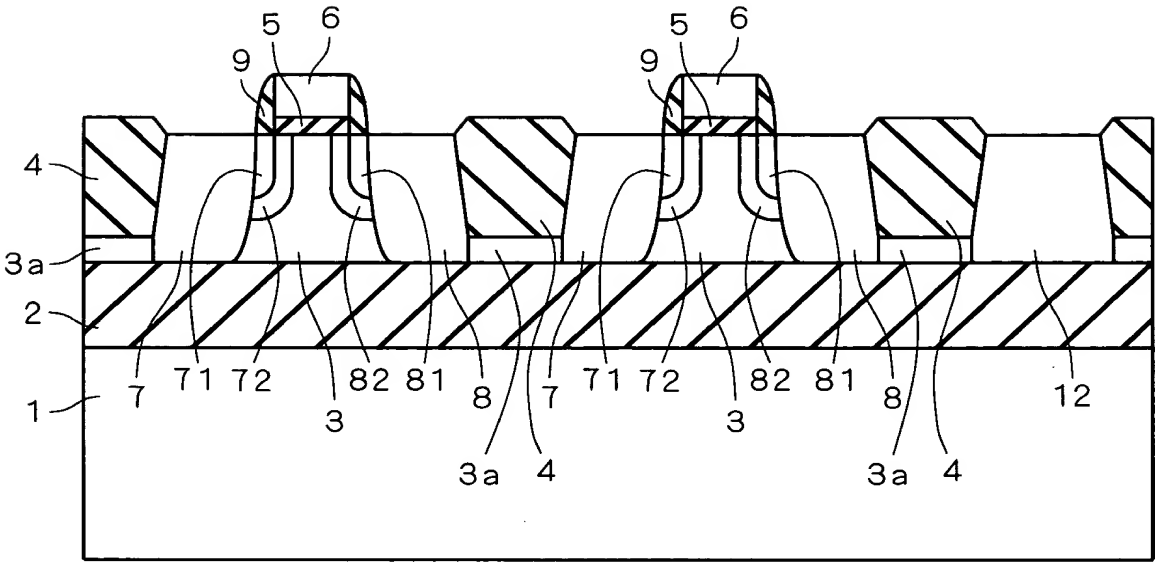
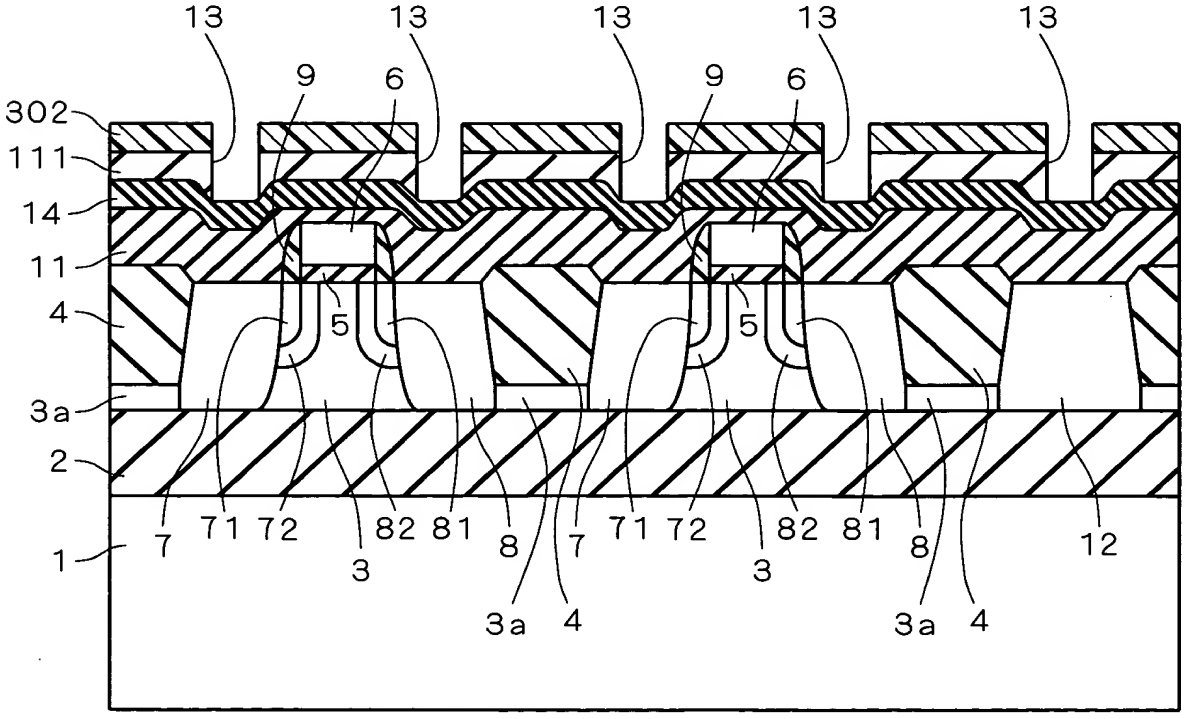

5
6
9
4
3a
2
1
7
71
72
3
82
81
8
3a
4
12

FIG. 13


13
9
6
302
111
14
11
4
5
3a
2
1
7
71
72
3
82
81
8
3a
4
12

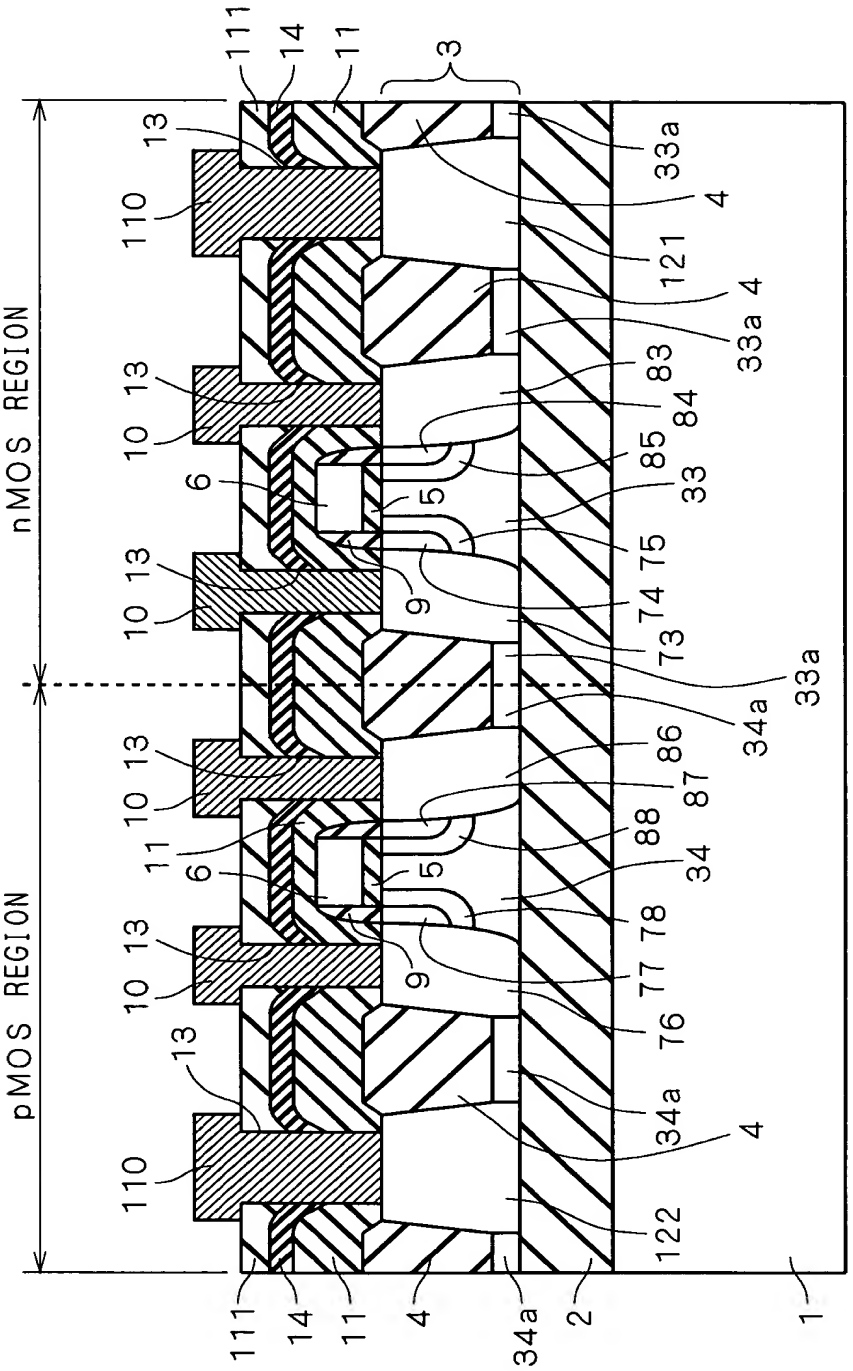
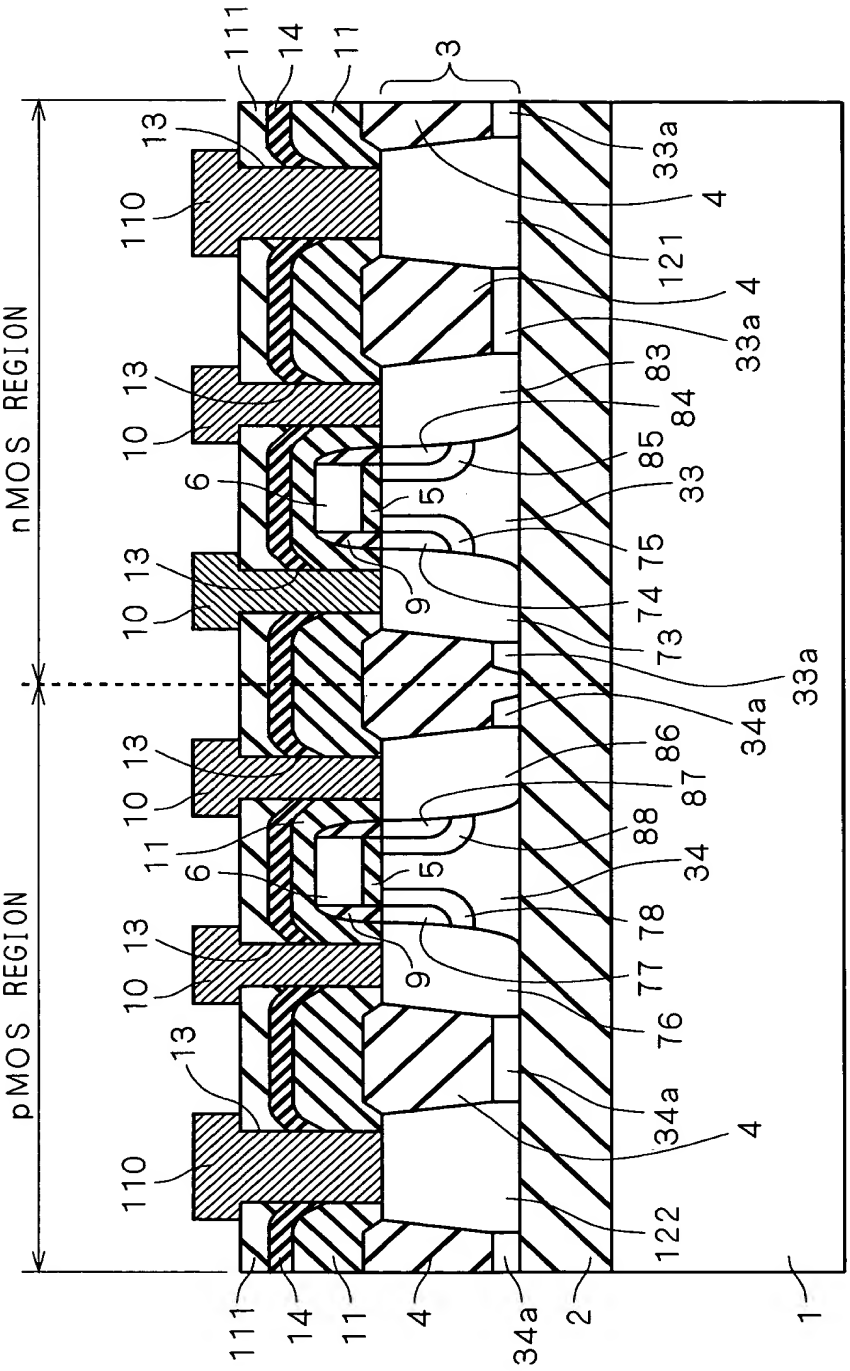

nMOS REGION
pMOS REGION
111
14
11
3
13
110
33a
4
121
83
84
85
33
10
6
5
9
75
74
73
34a
86
87
88
34
78
77
76
122
2
1

FIG. 14


nMOS REGION
pMOS REGION
111
14
11
3
13
110
33a
4
121
83
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85
33
10
6
5
9
75
74
73
34a
86
87
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77
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122
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1

FIG. 15

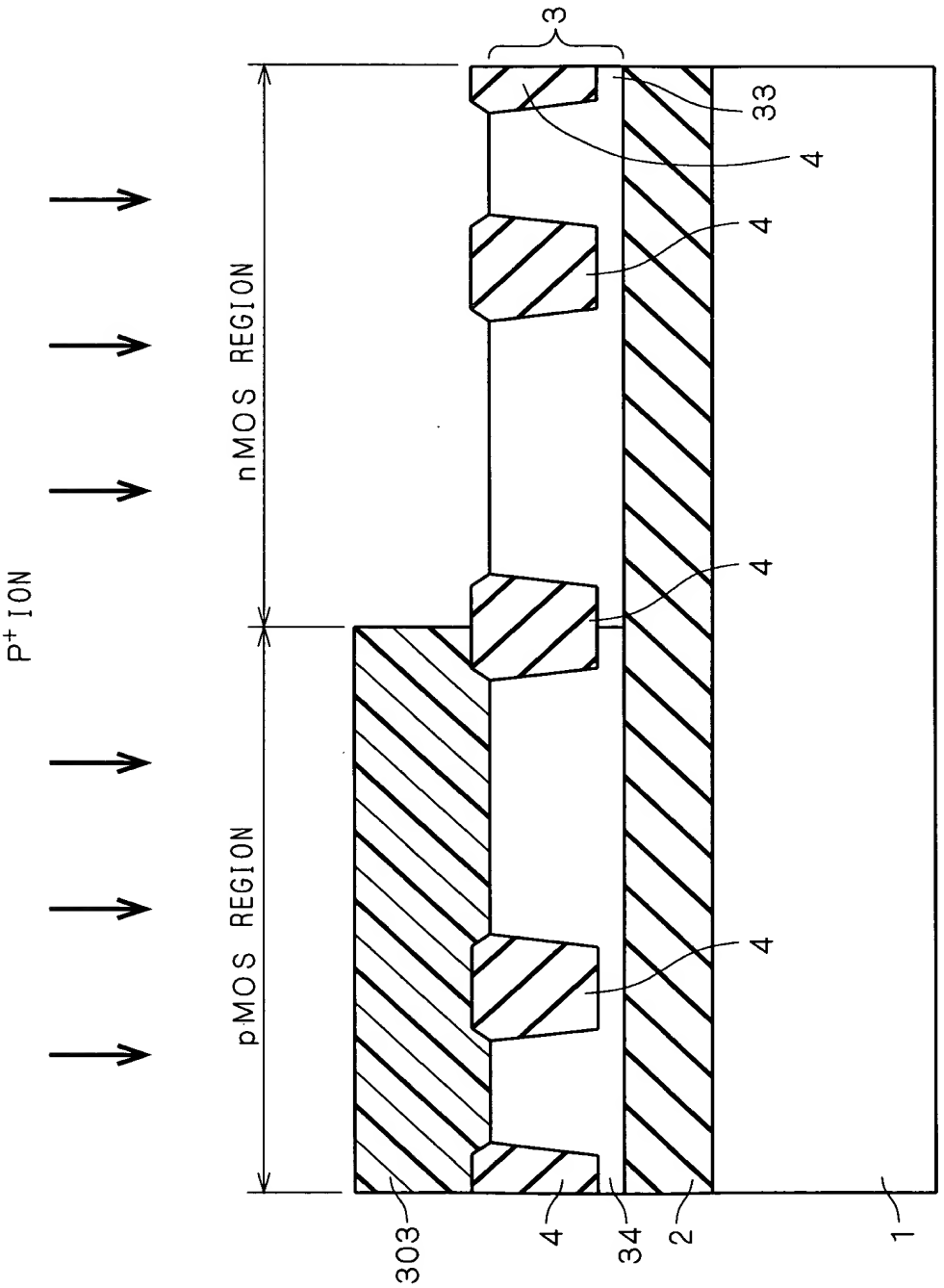
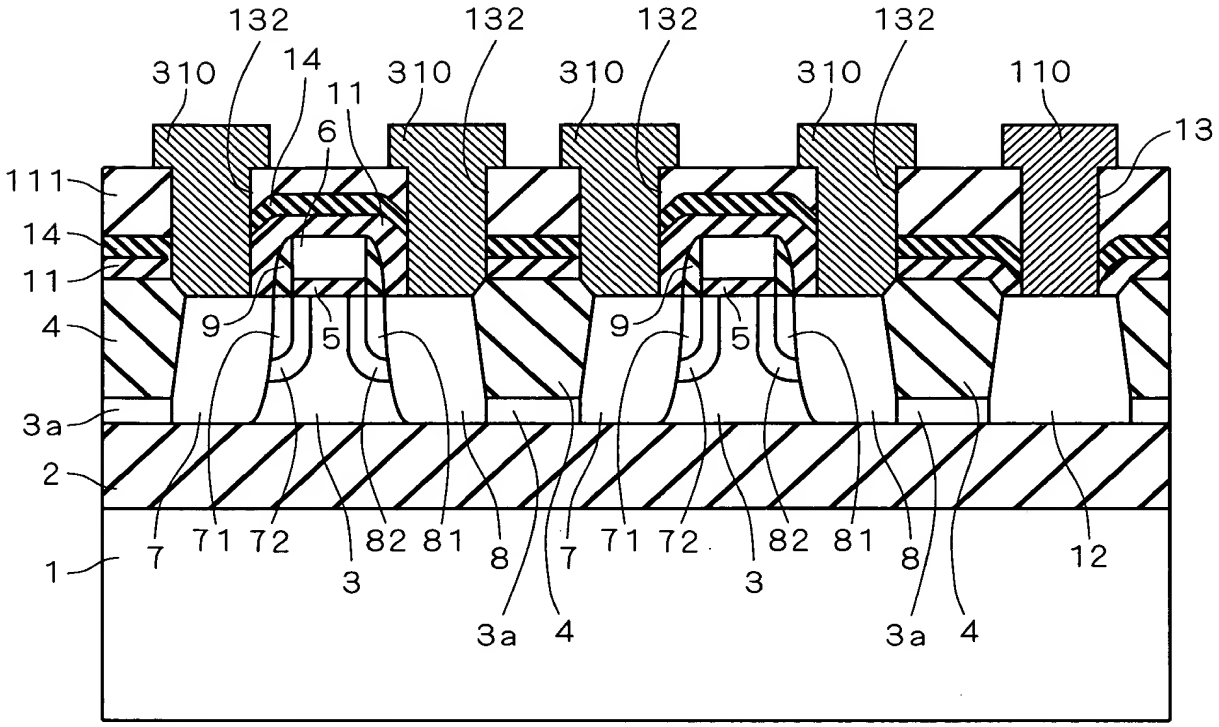


FIG. 16

FIG. 17


132
310
14
11
6
111
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11
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9
5
3a
2
1
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82
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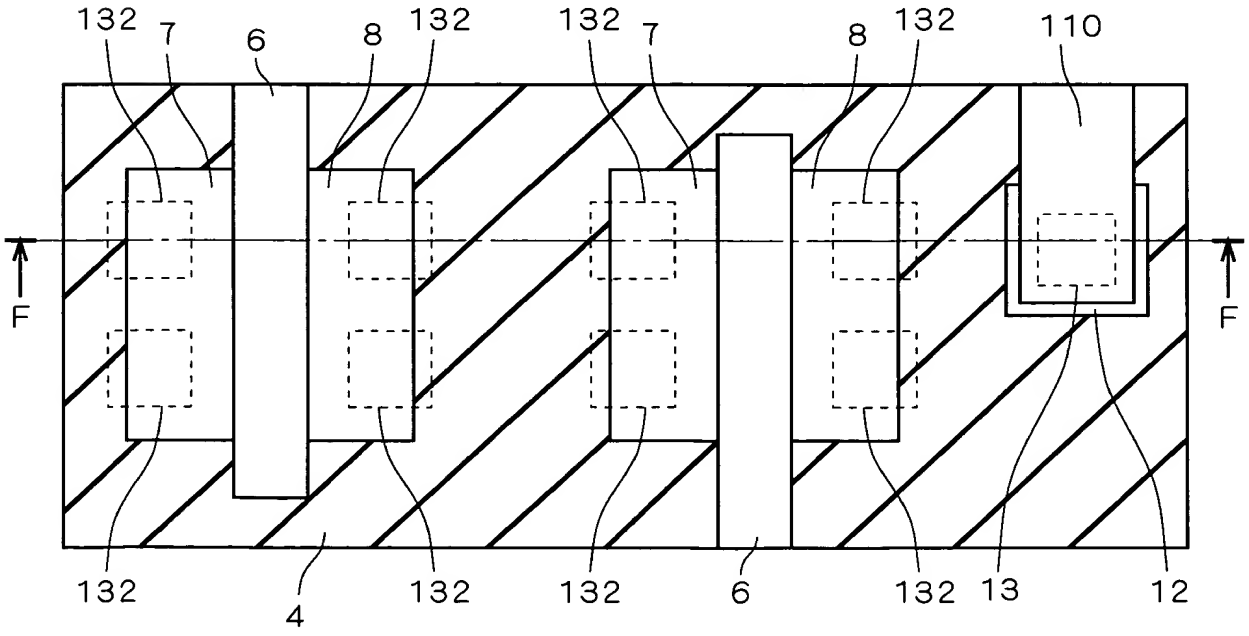
FIG. 18


132
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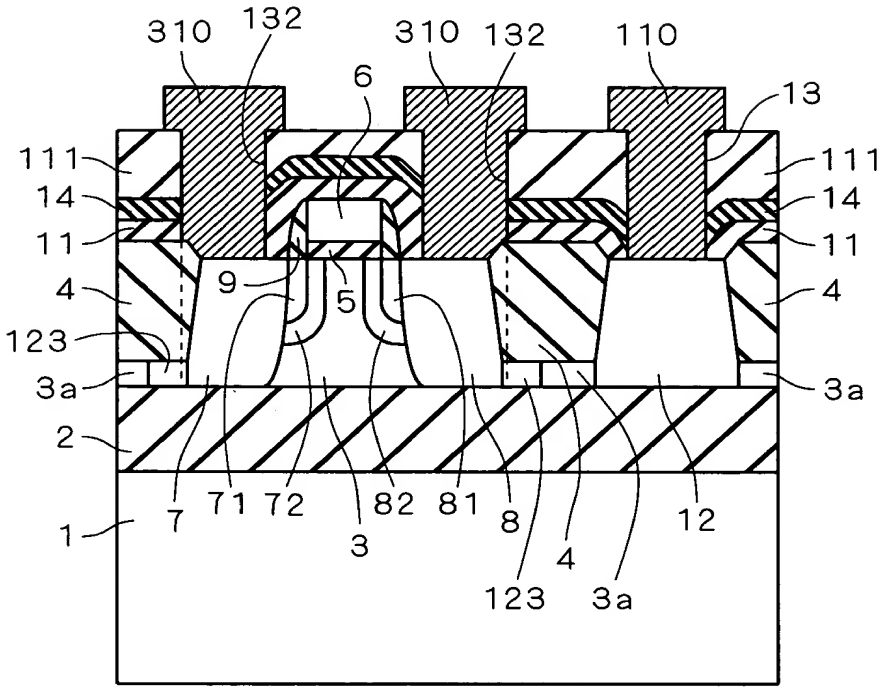
110

FIG. 19


310
132
310
132
110
6
13
111
111
14
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11
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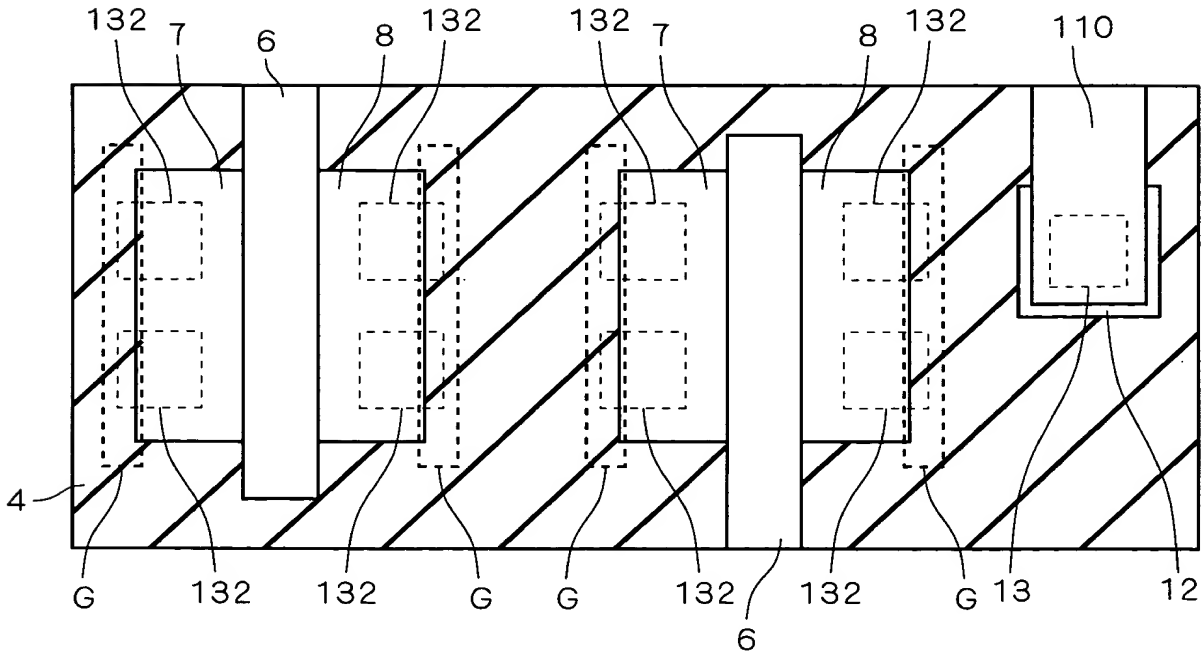
4
4
123
3a
3a
2
1
7
71
72
3
82
81
8
4
12
123
3a

FIG. 20


132
7
6
8
132
132
7
8
132
110
4
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132
132
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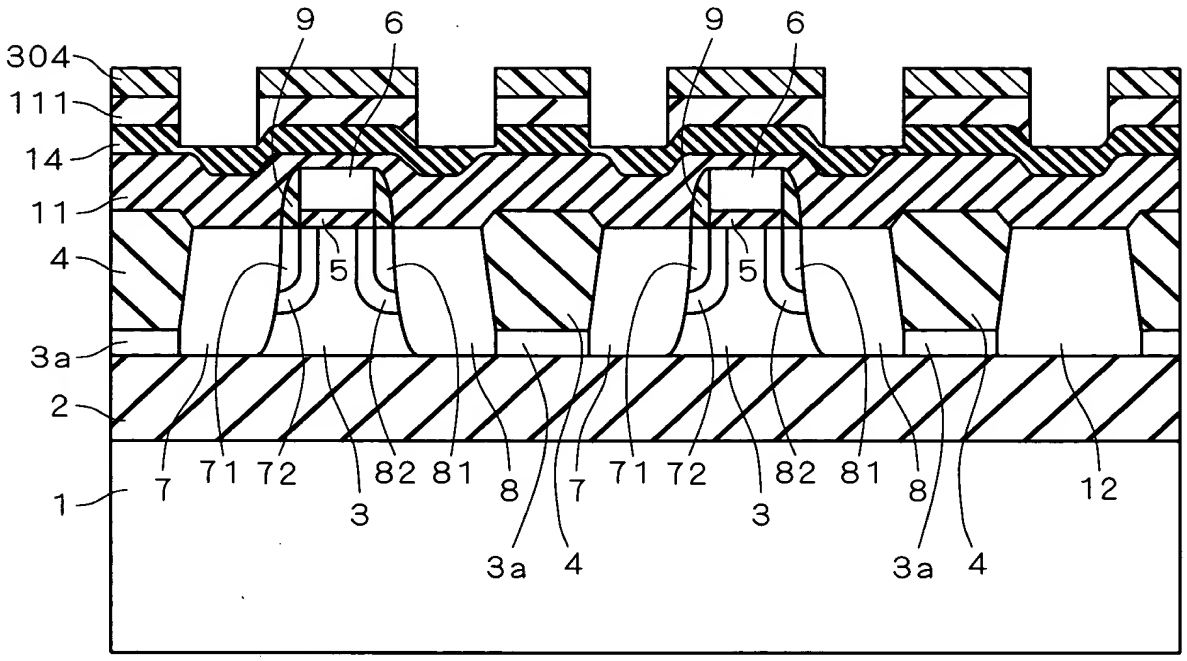
FIG. 21


304
111
14
11
4
3a
2
1
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6
5
7
71
72
3
82
81
8
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FIG. 22

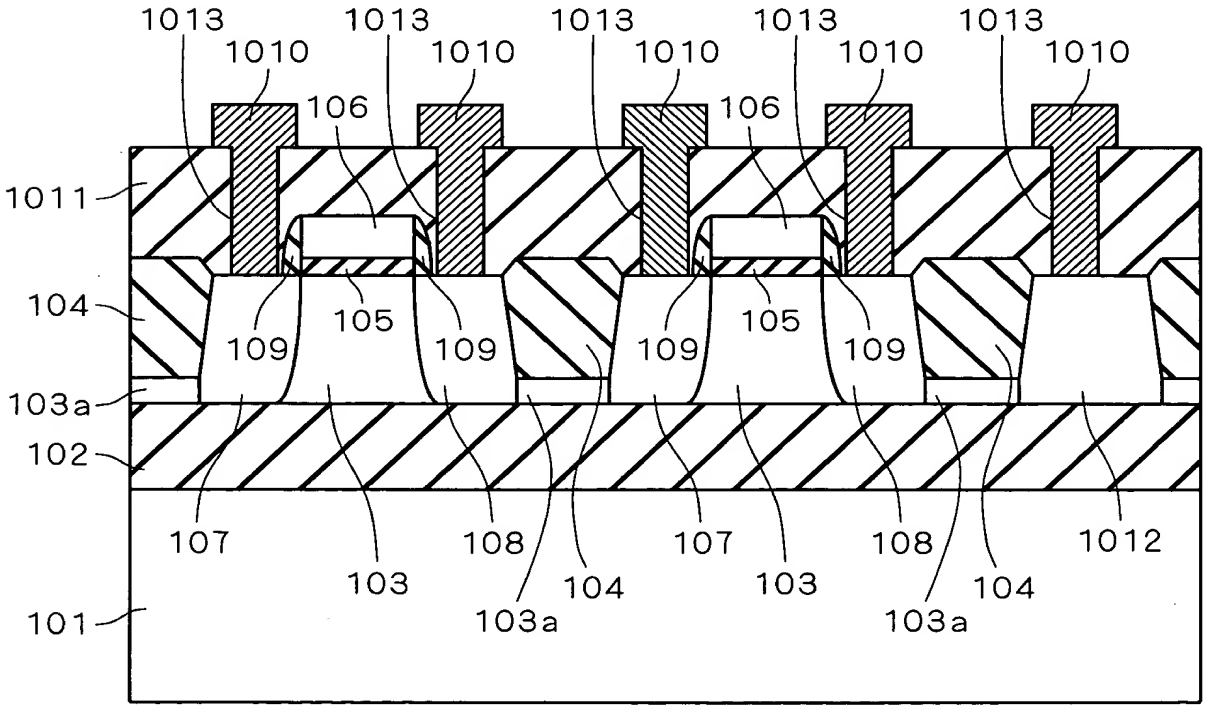
1013
1010
106
1011
104
109
105
103a
102
101
107
103
108
104
103a
1012

FIG. 23

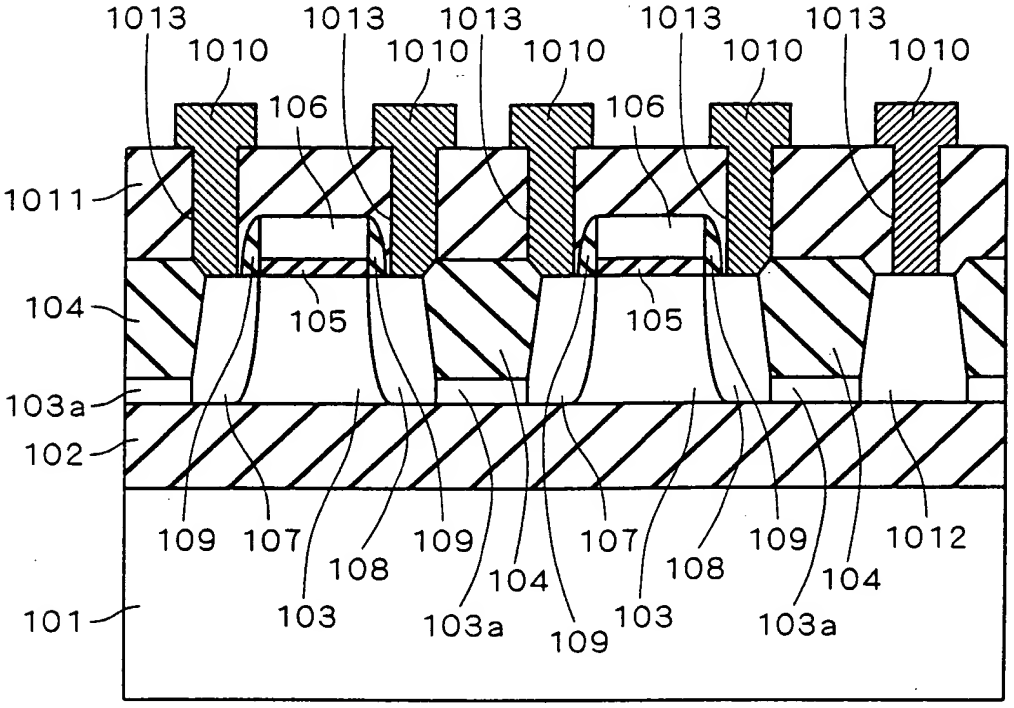
1013
1010
106
105
1011
104
103a
102
101
109
107
108
103
103a
104
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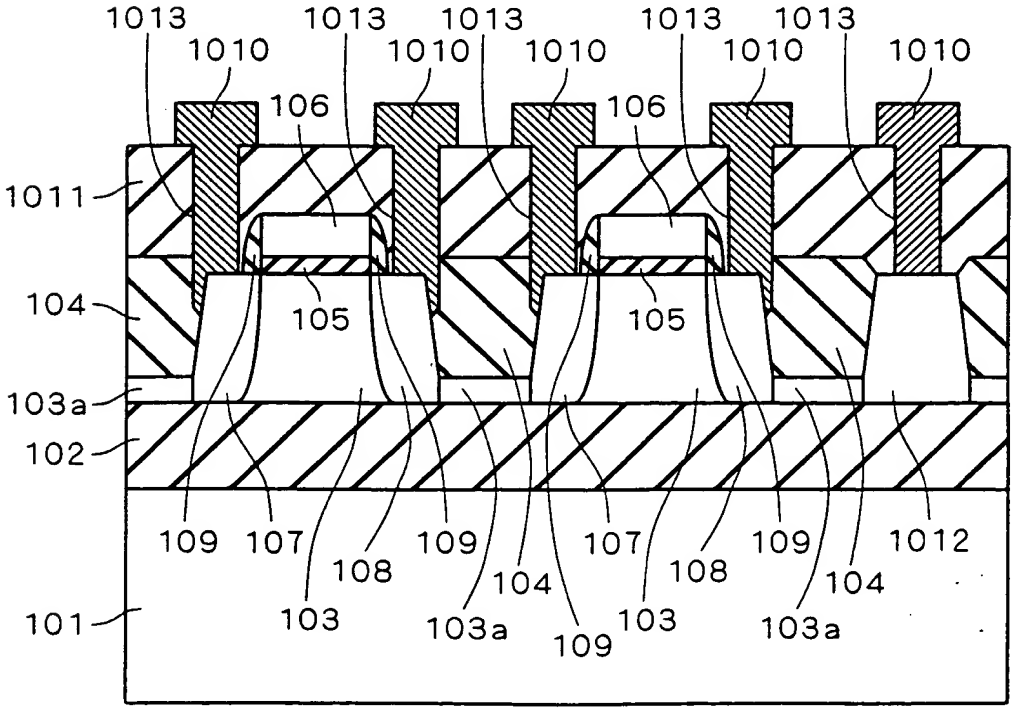
FIG. 24


1013
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106
105
1011
104
103a
102
101
109
107
108
103
103a
104
1012